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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/804,582	03/19/2004	Gerd Frankowsky	INFN/0072	7272
46798 7590 03/09/2007 PATTERSON & SHERIDAN, LLP Gero McClellan / Infineon / Qimonda 3040 POST OAK BLVD., SUITE 1500 HOUSTON, TX 77056			EXAMINER PATEL, PARESH H	
			ART UNIT	PAPER NUMBER
			2829	
SHORTENED STATUTORY PERIOD OF RESPONSE		MAIL DATE	DELIVERY MODE	
3 MONTHS		03/09/2007	PAPER	

**Please find below and/or attached an Office communication concerning this application or proceeding.**

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

<b>Office Action Summary</b>	<b>Application No.</b> 10/804,582	<b>Applicant(s)</b> FRANKOWSKY ET AL.	
	<b>Examiner</b> Paresh Patel	<b>Art Unit</b> 2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) ☒ Responsive to communication(s) filed on 21 December 2006.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) ☒ Claim(s) 1-30 is/are pending in the application.
- 4a) Of the above claim(s) 7-30 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-5 is/are rejected.
- 7) ☒ Claim(s) 6 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)                     | 4) <input type="checkbox"/> Interview Summary (PTO-413)           |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____                                      |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)          | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____  | 6) <input type="checkbox"/> Other: _____                          |

## **DETAILED ACTION**

### ***Election/Restrictions***

1. Applicant's election with traverse of Group I (claims 1-6) in the reply filed on 12/21/2006 is acknowledged. The traversal is on the ground(s) that switching devices of claims 1 and 7 have similar functions described in different manners. This is not found persuasive because different manner as claimed, makes different product as further stated in the last office action. Since different groups as stated in the last office action are different inventions, they requires different search and consideration, therefore it is burden on the PTO. However, upon allowance, if there is common allowable subject matter, Examiner will consider them for rejoining.

The requirement is still deemed proper and is therefore made FINAL.

### ***Response to Arguments***

2. Applicant's arguments filed 09/14/2006 have been fully considered but they are not persuasive. Examiner disagrees with Applicant for arguments about Koshikawa reference. Applicant argues that Koshikawa does not disclose testing and test circuit as claimed. Examiner disagrees because Koshikawa discloses claimed testing and test circuit. Here, broadest reasonable interpretation is given to all the limitations of claims including testing and a test circuit. Argument found at page 8 for "testing of the test circuit" is not true because in the claim it says, "testing of the first circuit".

Examiner again disagrees with Applicant for arguments about Schnabel reference. Applicant argues, Schnabel reference discloses that the test terminals are

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constantly connected to the memory 2 and therefore switching device is not selectively couple as claimed. Examiner respectfully disagrees because during testing switching device selectively connects the test terminal to the voltage line (not shown) of the memory 2. Also, an internal voltage line as argued here is inherent to the memory 2, because ordinary skill in the art knows that memory will only function with application of voltage, and internal wires that carries these voltage are the claimed internal voltage line. Since, claimed voltage line receives signal voltage during testing of the first circuit it reads on the memory 2 of Schnabel reference. Later, Applicant argues that Schnabel does not disclose activating a first switch to couple the test terminal to the internal voltage line after application of the activation signal. Examiner disagrees because "after" as mentioned here is not found in the claim.

***Claim Rejections - 35 USC § 102***

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-5 are rejected under 35 U.S.C. 102(b) as being anticipated by Koshikawa (US 5428299).

Regarding claim 1, Koshikawa in fig. 5 discloses an integrated circuit [21], comprising:

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a first circuit [26 (i.e. first and second voltage generating circuit) with 22] to be tested circuit comprising an internal voltage line [Vint];

a test circuit [23] for testing the first circuit;

a test terminal [Pext] coupled to the test circuit in order to provide an activation signal activating the test circuit to perform a test function; and

a switching device [24] to selectively couple the test terminal to the internal voltage line during testing of the test circuit [lines 55-68 of column 8 and fig. 6].

Regarding claim 2, Koshikawa discloses the integrated circuit of claim 1, wherein the test terminal is coupled to the internal voltage line to provide an electrical signal to the internal voltage line from an external source [Vext].

Regarding claim 3, Koshikawa discloses the integrated circuit of claim 1, wherein the switching device is further configured to isolate the test terminal from the test circuit after the activation of the test circuit [i.e. at Vext is lower, lines 3-12 of column 9].

Regarding claim 4, Koshikawa discloses the integrated circuit of claim 1, wherein the first circuit further comprises an internal voltage supply [step-down voltage generator 26].

Regarding claim 5, Koshikawa discloses the integrated circuit of claim 4, further comprising another switching device [25] responsive to the switching signal [EBL1] to selectively couple the internal voltage supply to the internal voltage line.

***Claim Rejections - 35 USC § 102***

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1-3 are rejected under 35 U.S.C. 102(e) as being anticipated by Schnabel (US 6788087).

The applied reference has a common assignee with the instant application.

Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

Regarding claim 1, Schnabel in fig.1-2 discloses an integrated circuit [1], comprising:

a first circuit [2] to be tested comprising an internal voltage line [voltage line of 2];  
a test circuit [3] for testing the first circuit;

a test terminal [5] coupled to the test circuit in order to provide an activation signal activating the test circuit to perform a test function [via 8] ; and

a switching device [11, 12 and 8] to selectively couple the test terminal to the internal voltage line during testing of the first circuit.

Regarding claim 2, Schnabel discloses the test terminal is coupled to the internal voltage line to provide an electrical signal to the internal voltage line from an external source [22].

Regarding claim 3, Schnabel discloses the switching device is further configured to isolate the test terminal from the test circuit after the activation of the test circuit [see Abstract].

### ***Claim Rejections - 35 USC § 103***

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

8. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Schnabel as applied to claim 1 above, and further in view of Horiguchi et al. (US 5347492).

Regarding claim 4, Schnabel discloses all the elements except for the first circuit further comprise an internal voltage supply. It would have been obvious to one having ordinary skill in the art at the time the invention was made to use internal voltage supply

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to operate partial circuit, since it was known in the art to reduce the power consumption of the integrated circuit [see lines 15-21 of column 1, US 5347492].

***Allowable Subject Matter***

9. Claim 6 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. See office action dated 09/15/2005 for reason for allowance.

***Conclusion***

10. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paresh Patel whose telephone number is 571-272-1968. The examiner can normally be reached on 8:00 to 4:30pm.



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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ha Nguyen can be reached on 571-272-1678. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



Paresh Patel  
Primary Examiner  
Art Unit 2829

March 05, 2007